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SIMULATION OF SEVEN LEVEL ASYMMETRIC MULTILEVEL INVERTER

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ABSTRACT

Multilevel inverters are popular in industry as it is providing more than two levels of voltages to achieve smoother and less distorted DC to AC power conversion. This paper presents seven level asymmetric multilevel inverter. This paper also presents the most relevant control and modulation method developed for this inverter: multicarrier pulse width modulation. Special attention is dedicated to the MATLAB simulation of H-bridge seven level multilevel inverter. Line to line and phase voltages are plotted using simulation. Finally FET analysis is carried out to find total harmonic distortion.

KEYWORDS: Multilevel Inverters, Power Converters, H-Bridge Inverters

INTRODUCTION

Power-electronic inverters are becoming popular for various industrial drives applications. It is necessary that the output voltage waveform of an ideal inverter should be sinusoidal. The voltage waveforms of practical inverters are, however, non-sinusoidal and contain certain harmonics. Square wave or quasi-square wave voltage may be acceptable for low and medium power applications but for high power applications low distorted sinusoidal waveform are required. Multilevel inverters have gained popularity in high power applications due to their low switching frequency, low harmonics and modularity.

Today these inverters are considered as the most suitable power converters for high-voltage-capability and high-power-quality demanding applications. Lower common-mode voltages, near-sinusoidal outputs, together with small *dv/dt*'s, are some of the characteristics that have made these power converters popular for industry and research [4]. Multi-level inverters can operate not only with PWM techniques but also with amplitude modulation (AM), improving significantly the quality of the output voltage waveform. With the use of amplitude modulation, low frequency voltage harmonics are perfectly eliminated, generating almost perfect sinusoidal waveforms, with a THD lower than 5 % [5].

The main advantages of multilevel inverters are

- Low harmonic distortion of the generated output voltage
- Low electromagnetic emissions.
- High efficiency.
- Capability to operate at high voltages, and modularity.

Each converter operated at a low switching frequency, reducing the semiconductor stresses, and therefore reducing the switching losses. The development of multilevel inverters over the last decades has matured into three widely accepted topologies:

- Neutral point clamped (NPC)
- Flying capacitor (FC)

- Cascaded H-bridge inverter.

MULTILEVEL INVERTER

The principal function of the inverters is to generate an ac voltage from a dc source voltage. If the dc voltage is composed of many small voltage sources connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and *dc* voltage sources required to generate a stair case output voltage waveform. The H-bridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source *Vdc*. By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced. Figure 1 provides an illustration of a single-phase cascaded H-bridge multilevel inverter using 3-SDCSs [8]. By closing the appropriate switches, each H-bridge inverter can produce three different voltages: +*Vdc*, 0 and -*Vdc*.

As mentioned earlier, each H-bridge inverter produces an AC voltage *vi*, where *i* stands for one particular H-bridge inverter. Figure 1 contains three such H-bridges, one for each DC source. Therefore, to obtain the total AC inverter phase voltage, these three distinct AC voltages are added together [7].

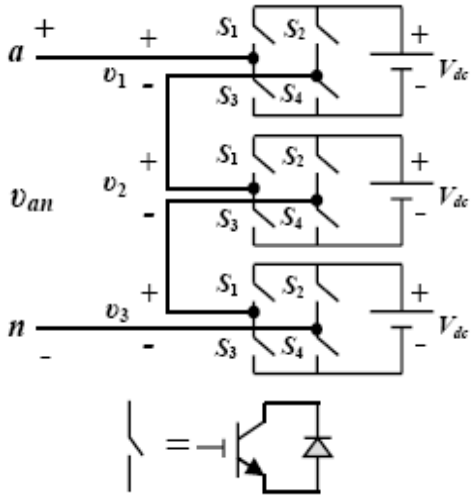

Figure 1: H-Bridge Multilevel Inverter Using 3-SDCS

Figure 2 provides an illustration of these ideas [8]. It also illustrates the idea of "levels" in a cascaded H-bridges multilevel inverter. The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a 3-level waveform, a single full-bridge inverter is employed. In Figure 2, one notices that three distinct DC sources ($s = 3$, where s is the number of DC sources) can produce a maximum of ($l = 7$ distinct levels) in the output phase voltage of the multilevel inverter. More generally, a cascaded H-bridge multilevel inverter using s - SDCSs can produce a maximum number of levels given by the equation:

$$l = (2s + 1) \quad (1)$$

Where, l is the distinct number of levels in the output phase voltage.

And s is the number of SDCSs

The concept of cascaded multilevel inverter with SDCSs is very interesting due to many reasons. This topology requires the least number of components, among all multilevel inverters, to achieve the same number of voltage levels. It is also possible to modularize circuit layout and packaging because each level has the same structure, and there are no extra

clamping diodes or voltage balancing capacitors. In addition, soft switching technique can be applied in this structure to avoid bulky and resistor-capacitor-diode snubbers with losses, as part of future work.

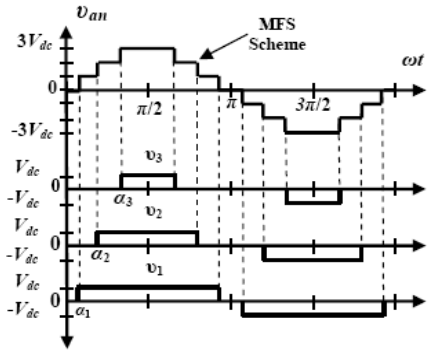

Figure 2: Output Voltage of H-Bridges 7-Level Inverter

Multilevel inverters are implemented with small dc sources, used to form a stair case ac waveform, which follows a given reference template. The AC voltage waveform resulting produced from these DC voltages is approximately sinusoidal. By switching the DC voltages to the AC output, a staircase (stepped) waveform can be produced which approaches the sinusoidal waveform with minimum THD. The waveforms are of better harmonic spectrum and attain higher voltages with a limited maximum device rating.

ASYMMETRIC MULTILEVEL INVERTER

In all the well-known multilevel converter topologies, the number of power devices required depends on the output voltage level needed. However, increasing the number of power semiconductor switches also increases converter circuit and control complexity and cost. To provide a large number of output levels without increasing the number of converters, asymmetric multilevel converters (AMC) can be used.

Traditionally, each phase of a cascaded multilevel inverter requires ‘n' dc sources for 2n+1 levels. For many applications, it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H- bridge multilevel inverter, an asymmetric topology is proposed as shown in Figure 3. This provides the capability to produce higher voltages at higher speeds with low switching frequency.

Figure 4 shows a detail of the partial cells and the main notations used. Each couple of switches *S jx* and *S ' jx* (x = 1,2; j = 1..K) is controlled by a couple of switching functions

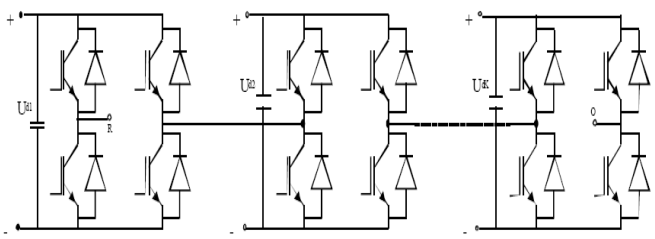

Figure 3: Series-Connected Inverters Topology with *K* Cells per Phase

M jx andM ' jx $\in$ {0,1}

The output voltage of each cell is given by

$$Upj=Fj*Udj, Upj \in \{-Udj, 0, Udj\} \quad (2)$$

Equation 2 shows that each partial cell can generate three different levels. The output voltage of the multilevel converter is given by :

$$Us = U_{p1}+U_{p2}+..+U_{pK} \quad (3)$$

A series-connected multilevel inverter is known as asymmetric, if at least one to the dc voltage sources feeding the partial inverters is different of the others. Three conditions have been established for the design of a regular step AMI :

The dc-voltage sources must be arranged in an increasing way

$$U_{d(h-1)} \leq U_{dh}, \quad \forall h=2\ldots K; \quad (4)$$

The ratio between two consecutive inverters must be an integer

$$U_{dh}/U_{d(h-1)} = \delta_h, \ \delta_h \in N^* ; \quad (5)$$

The jth partial cell must be fed by the voltage *U dj* such that

$$U_{dj} \leq 2\left(\sum_{l=1}^{j-1} \boldsymbol{Udl}\right) + 1 \quad (6)$$

If these three conditions are satisfied, the multilevel inverter will generate an output voltage *Us* with *N* regular different levels.

The DCVS levels can be chosen according to a geometric progression with a factor of two or three. Equations 7 and 8 summarize the relationships between *N* and *K*. These approaches are only two particular cases.

$$N = 2^{(K+1)} - 1 \text{ if } U_{dj} = 2^{(j-1)}.U_{d1} \quad (7)$$

$$N = 3^K \text{ if } U_{dj} = 3^{(j-1)}.U_{d1} \quad (8)$$

This approach allows to take accurately into account the particularity of power devices and the other design constraints. It provides more flexibility due to its easy expansion, and a large number of degrees of freedom to the designer.

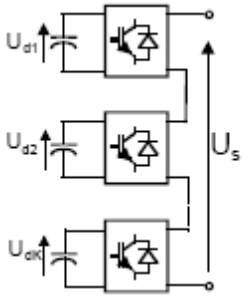

Figure 4: Partial Cells Used

TOTAL AND PARTIAL ASYMMETRY FACTORS

The first fundamental concept of asymmetric multilevel converters is based on the fact that the DC voltages U_{dj} (j = 1….K) supplying each partial inverter are a ratio of the equivalent total DC-link voltage of the converter, *Ue*. These ratio factors are denoted λ_j and are called the total asymmetry factors.

$$\lambda_j = \frac{\mathbf{Ue}}{\boldsymbol{Udj}}, \ \forall \ j = 1 \ K \quad (9)$$

The equivalent total DC-link voltage *Ue* is given by the following relationship:

$$U_e = 2 \sum_{j=1}^{K} \mathbf{Udj} \quad (10)$$

The second fundamental concept is based on the ratio between DC-voltages supplying consecutive partial inverters. These ratio factors are denoted δ_h ($h = 2..K$) and are called partial asymmetry factors.

$$\delta_h = \frac{Udh}{Ud(h-1)}, \forall \mathbf{h = 2 \quad K} \tag{11}$$

The advantages of asymmetric topology are:

- The number of separate DC supplies used is reduced in this configuration.
- Due to the different input voltages of the cells, high-voltage switches presenting low relative conduction losses are combined with low-voltage switches having low commutation time. Naturally, for most operating points, the switching frequency of low voltage cells is higher. Thus low output switching frequency is required.
- Low switching losses occur as the number of semiconductor devices is reduced.
- From the voltage resolution point of view, with the same number of cells, the asymmetrical multilevel inverter allows a higher resolution than symmetrical multilevel inverters. In the symmetrical case, the number of levels grows proportionally to the number of cells, in the asymmetrical case, it grows exponentially.
- High conversion efficiency is achieved.
- Flexibility to enhance the performance using various control strategies are possible.
- Reduction in complexity and cost is achieved due to lesser number of semiconductor devices and hence simpler commutation and triggering circuits.
- One major demerit of asymmetric configuration is that the cells have to be insulated from each other; this constitutes the major complexity of these structures.

SEVEN LEVEL ASYMMETRIC INVERTER

In seven-Level Asymmetrical Inverter each leg of a single phase contains 2 DCVS (DC Voltage Source) of 100V and 200V unlike the 3 DCVS of 100V each in 7-Level Symmetrical Inverter. This arrangement thus reduces the number of voltage supplies used. Also the number of IGBTs used is only 24 unlike 36 in the symmetric configuration. Here too the H-Bridge topology is used. Each H-Bridge has 4 IGBTs in it. And each leg has 2 such H-Bridges. To prevent commutation errors, same switching pulses are provided to IGBT (1, 2), (3, 4), (5, 6), (7, 8) and so on in the other two phases as well. Due to the different input voltages of the cells, high-voltage switches presenting low relative conduction losses are combined with low-voltage switches having low commutation time. Naturally, for most operating points, the switching frequency of low voltage cells is higher. Together with the switch characteristics, one can take advantage of this specificity. The three legs are star connected and neutral is earthed. Imports are connected to all IGBTs to provide switching pulses. Three connection ports are provided in all three phases, namely, A, B and C. These ports are provided to carry out voltage measurements, namely, line voltage and the phase voltages. Subsystem of this is created and the arrangement is as shown in Figure 7.

The Pulse generation circuit that employs the pulse width modulation technique with switching frequency of low voltage cells being higher than that of high voltage cells [14]. The waveforms of the triangular carrier waves and the sinusoidal reference wave are shown in Figure 5. Figure 6 shows the pulse train generated. The line-line voltage and the phase voltage are shown in Figure 8 and Figure 9 respectively. The *powergui* block is used to carry out the FFT analysis which is shown in Figure 10. The THD comes out to be 12.97% in the asymmetrical configuration.

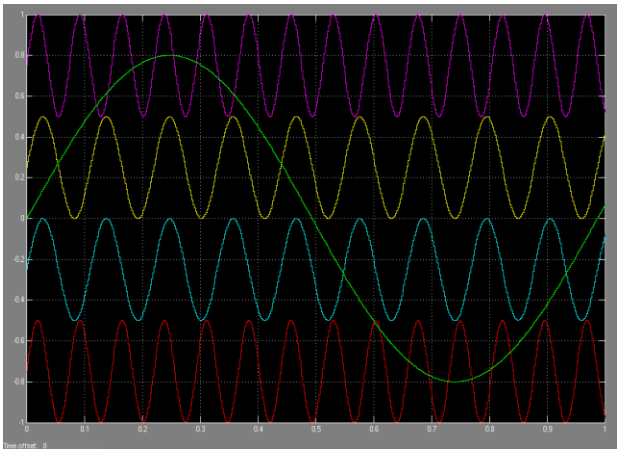

Figure 5: Waveforms of Carrier and Reference Waves for Asymmetric Configuration

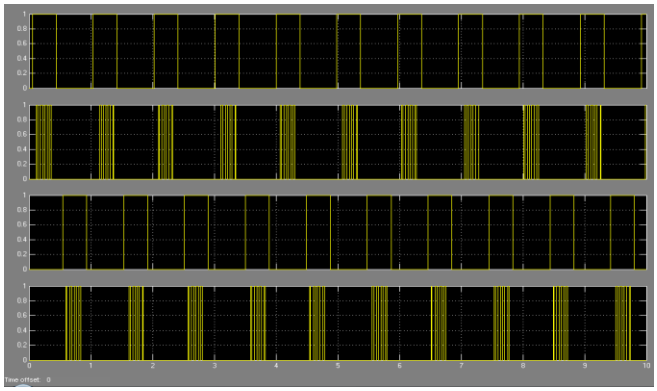

Figure 6: Pulse Train for Asymmetric Configuration

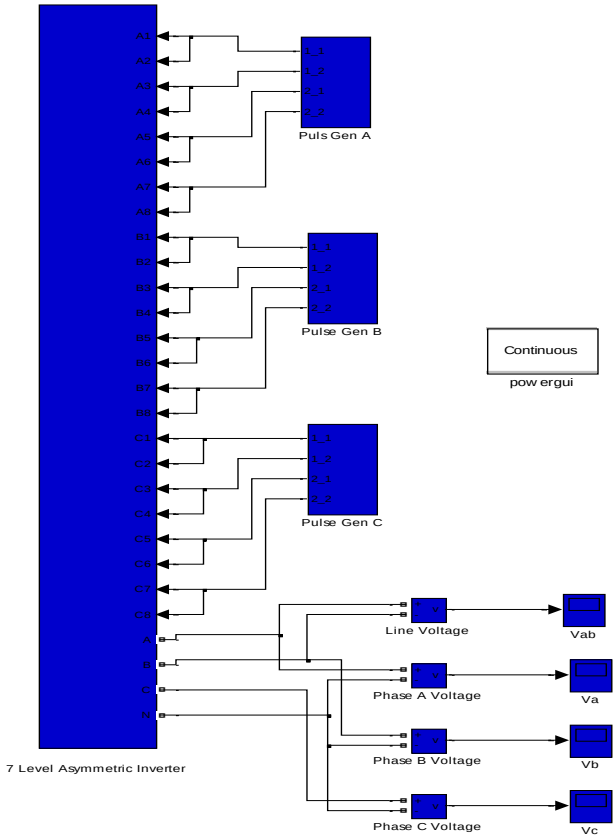

Figure 7: Simulated 7-Level Asymmetric Inverter Circuit

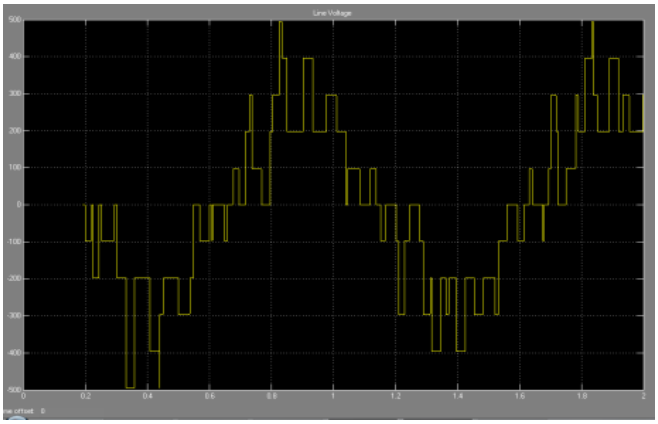

Figure 8: Line-Line Voltage Waveform of Asymmetrical Configuration

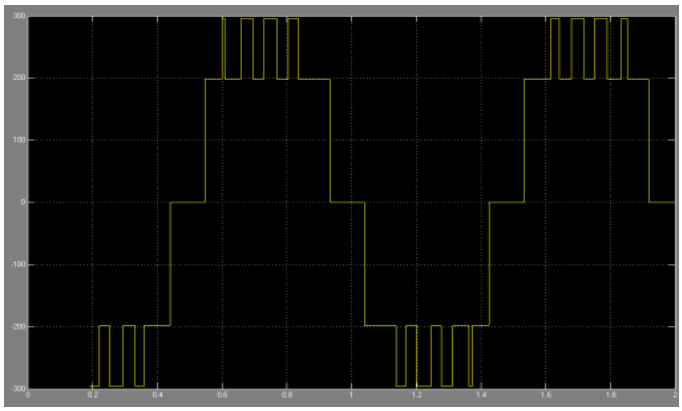

Figure 9: Phase Voltage Waveform of Asymmetrical Configuration

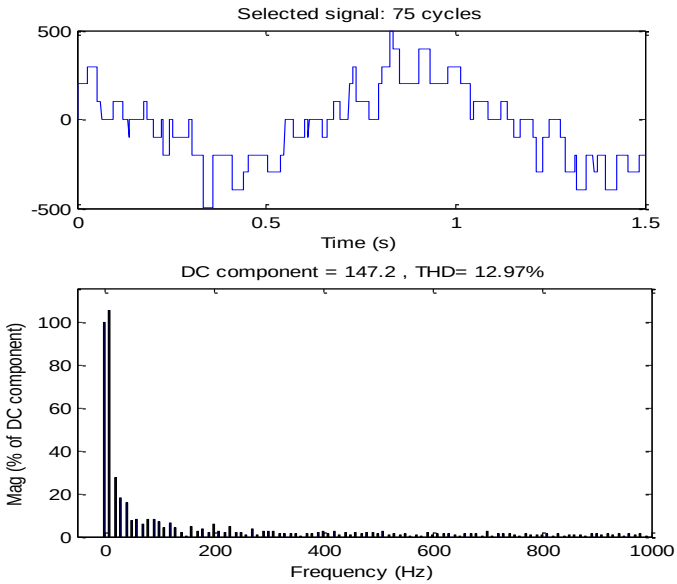

Figure 10: The FFT Analysis of the Asymmetrical Configuration

CONCLUSIONS

The modeling of 7-level asymmetric inverter was done and simulated using MATLAB/SIMULINK. The total harmonic distortion (THD) of the asymmetric configuration was found to be only 12.97%, which is much lesser than that of the conventional configuration. The simulation result shows that the harmonics have been reduced considerably. The 7-level asymmetric inverters have been successfully simulated and the results of line-line voltage waveforms, phase

voltage waveforms and the FFT analysis are obtained. The inverter system can be used in industries for the adjustable speed drives and significant amount of energy can be saved as the system has less harmonic losses.

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